# Claims

[c1] A method for forming a memory storage cell in a semiconductor substrate, the method comprising:
forming a dopant source material over a lower portion of a deep trench formed in the substrate;
shaping an upper portion of the trench to a generally rectangular configuration; and
annealing said dopant source material so as to form a buried plate of a trench capacitor;
wherein said buried plate is self aligned to said shaped upper portion of the trench.

[c2] The method of claim 1, wherein said shaping an upper portion of the trench is implemented through an ammonia etch, said ammonia etch having an etch rate selective to a crystal orientation of the substrate material.

[c3] The method of 1, wherein said dopant source material comprises arsenic doped oxide (ASG).

[c4] The method of claim 3, further comprising forming a cap layer over said ASG layer following said shaping an upper portion of the trench.

[c5] The method of claim 1, wherein said annealing said dopant source material is implemented at about 1050 °C for about 3 minutes.

[c6] The method of claim 1, wherein said forming a dopant source material over a lower portion of a deep trench formed in the substrate further comprises:
depositing said dopant source material over the trench sidewall and lower surfaces;
filling said trench with a photoresist material and recessing said photoresist material to a desired depth; and
etching a portion of said dopant source material on an upper part of the trench, wherein said recessed photoresist serves as an etch stop layer.

[c7] The method of claim 6, further comprising:
removing the remaining photoresist material from said lower portion of said deep trench;
performing a thermal annealing so as to cause said dopant source material to diffuse into the substrate; and
removing said dopant source material and a cap layer formed over said dopant source material.

[c8] The method of claim 7, wherein said annealing said dopant source material is implemented at about 1050 °C for about 3 minutes.

[c9] The method of claim 8, wherein said annealing is performed in an oxygen-containing atmosphere.

[c10] The method of claim 7, wherein said removing said dopant source material and said cap layer is implemented by at least one of a buffered hydrofluoric (BHF) etch and a diluted hydrofluoric (DHF) etch.

[c11] A method for forming vertical storage cell for a dynamic random access memory (DRAM) device, the method comprising:
forming a deep trench in a semiconductor substrate;
forming a dopant source material over a lower portion of said deep trench;
shaping an upper portion of said deep trench to a generally rectangular configuration; and
annealing said dopant source material so as to form a buried plate of a trench capacitor;
wherein said buried plate is self aligned to said shaped upper portion of said deep trench.

[c12] The method of claim 11, wherein said shaping an upper portion of said deep trench is implemented through an ammonia etch, said ammonia etch having an etch rate selective to a crystal orientation of the substrate material.

[c13] The method of 11, wherein said dopant source material comprises arsenic doped oxide (ASG).

[c14] The method of claim 13, further comprising forming a cap layer over said ASG layer following said shaping an upper portion of said deep trench.

[c15] The method of claim 11, wherein said annealing said dopant source material is implemented at about 1050 °C for about 3 minutes.

[c16] The method of claim 11, wherein said forming a dopant source material over a lower portion of said deep trench formed in the substrate further comprises:
depositing said dopant source material over the trench sidewall and lower surfaces;
filling said deep trench with a photoresist material and recessing said photoresist material to a desired depth; and
etching a portion of said dopant source material on an upper part of said deep trench, wherein said recessed photoresist serves as an etch stop layer.

[c17] The method of claim 16, further comprising:
removing the remaining photoresist material from said lower portion of said deep trench;
performing a thermal annealing so as to cause said

dopant source material to diffuse into the substrate; and removing said dopant source material and a cap layer formed over said dopant source material.

[c18] The method of claim 17, wherein said annealing said dopant source material is implemented at about 1050 °C for about 3 minutes.

[c19] The method of claim 18, wherein said annealing is performed in an oxygen-containing atmosphere.

[c20] The method of claim 7, wherein said removing said dopant source material and said cap layer is implemented by at least one of a buffered hydrofluoric (BHF) etch and a diluted hydrofluoric (DHF) etch.

[c21] A semiconductor memory storage cell, comprising:
a deep trench initially formed in a semiconductor substrate;
a buried plate region formed in a lower portion of said deep trench; and
an upper portion of said deep trench being shaped to have a generally rectangular shape following the initial formation thereof;
wherein said buried plate region is self aligned with said shaped upper portion of said deep trench.

[c22] The memory storage cell of claim 21, wherein said

buried plate region is formed by an anneal of a dopant source material formed over said lower portion of said deep trench, wherein said dopant source material is further used to shield said lower portion of said deep trench during the shaping of said upper portion of said deep trench.

[c23] A buried plate region for a semiconductor memory storage capacitor, wherein said buried plate region is self aligned with respect to an upper portion of a deep trench containing said memory storage capacitor.

[c24] The method of claim 5, wherein said annealing is performed in an oxygen-containing atmosphere.

[c25] The method of claim 15, wherein said annealing is performed in an oxygen-containing atmosphere.